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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,348	06/10/2005	Christophe Joly	PHUS020583	3789

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EXAMINER
NGUYEN, HIEU P

ART UNIT	PAPER NUMBER
2817	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,348	JOLY ET AL.	
	Examiner	Art Unit	
	Hieu P. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

The specification has not been checked to the extent necessary to determine the presence to all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-14 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim1-18 of copending Application No.

10,538,347. Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications similarly claim an amplifier comprising: a circuit means and a detector circuit means.

Regarding claim 1 and 3,

Joly's **claim 1** recites:

1. A radio frequency (RF) linear power amplifier (200) operating in an output frequency band, having an output transistor (Q2), said power amplifier comprising:

(a) **a circuit means (300')** for generating a bias signal producing a quiescent current flowing through said output transistor (Q2) of said RF power amplifier,

(b) **a detector circuit means (210)** for detecting RF input to said amplifier and generating a driving signal (215) according to a power level of said RF input;

(c) **a self-adapting circuit means (250)** for receiving said driving signal (215) and automatically modifying said bias signal and said quiescent current through said output transistor (Q2), whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels (note: the self-adapting circuit means can be read as "**a sliding bias circuit**" in claim 3).

Joly's **claim 13** also recites:

a self-adapting circuit (250) for dynamically controlling quiescent current flowing through said output transistor of a linear power amplifier operating in an output frequency band, having an output transistor, said linear power amplifier comprising **a circuit means (300')** for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said self-adapting bias circuit comprising:

a) **a detector circuit means (210)** for detecting RF input to said amplifier and generating a driving signal (215) according to a power level of said RF input;

b) means (225, 228) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

Regarding claim 2, Joly's **claim 16** recites:

The self-adapting circuit as claimed in claim 13, wherein said circuit means for generating a bias signal producing a quiescent current comprises **a differential transistor pair** (325), said modifying means is connected to one side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

Regarding claim 4, Joly's claim 4 recites:

The linear power amplifier as claimed in claim 2, wherein the self adapting circuit means (250) **includes means (225, 228)** for automatically reducing the quiescent current for an output stage amplifier from one state of lower quiescent current to another state of higher quiescent current.

Regarding claim 5, Joly's claim 5 recites:

The linear power amplifier as claimed in claim 1, comprising first and second power output stages, wherein said detector circuit means (210) detects RF input to said amplifier at said first output stage (Q1), for reducing said quiescent current at a second output stage (Q2).

Regarding claim 6, Joly's claim 6 recites:

The linear power amplifier as claimed in claim 1, further comprising means (125, 126) for further modifying said quiescent current at a second output stage under discrete voltage control.

Regarding claims 7 and 9:

Joly's claim 8 recites:

A device (communication device) including a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor, said power amplifier comprising:

(a) **a circuit means (300')** for generating a bias signal producing a quiescent current flowing through said output transistor (Q2) of said RF power amplifier;

(b) **a detector circuit means (210)** for detecting RF input to said amplifier and generating a driving signal (215) according to a power level of said RF input;

(c) **a self-adapting circuit means (250)** for receiving said driving signal (215) and automatically modifying said bias signal and said quiescent current through said output transistor (Q2), whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

Joly's **claim 13** also recites:

a self-adapting circuit (250) for dynamically controlling quiescent current flowing through said output transistor of a linear power amplifier operating in an output frequency band, having an output transistor, said linear power amplifier comprising **a circuit means (300')** for

generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said self-adapting bias circuit comprising:

a) **a detector circuit means (210)** for detecting RF input to said amplifier and generating a driving signal (215) according to a power level of said RF input;

b) means (225, 228) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels (note: the self-adapting circuit means can be read as "**a sliding bias circuit**" in claim 9).

Regarding claim 8, Joly's **claim 16** recites:

The self-adapting circuit as claimed in claim 13, wherein said circuit means for generating a bias signal producing a quiescent current comprises **a differential transistor pair** (325), said modifying means is connected to one side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

Regarding claim 10, Joly's claim 12 recites:

The device as claimed in claim 7, further comprising means (125, 126) for further modifying said quiescent current at a second output stage under discrete voltage control.

Regarding claim 11, Joly's claim 13 recites:

A self-adapting circuit (sliding bias circuit) for dynamically controlling quiescent current flowing through said output transistor of a linear power amplifier operating in an output frequency band, having an output transistor, said linear power amplifier comprising a circuit

means (300') for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said self-adapting bias circuit comprising:

a) **a detector circuit means (210)** for detecting RF input to said amplifier and generating a driving signal (215) according to a power level of said RF input;

b) means (225, 228) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

Regarding claim 12, Joly's claim 14 recites:

The self-adapting circuit as claimed in claim 13, wherein said circuit means for generating a bias signal producing a quiescent current comprises **a differential transistor pair** (325), said modifying means is connected to one side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

Regarding claim 13, joly's claim 17 recites:

The self-adapting circuit as claimed in claim 13, wherein said linear power amplifier comprises first (Q1) and second (Q2) power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage, for reducing said quiescent current at a second output stage (Q2).

Regarding claim 14, Joly's claim 1 recites:

The self-adapting circuit as claimed in claim 13, wherein said second power output stage firer includes **means (125, 126)** for further modifying said quiescent current at a second output stage under discrete voltage control.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 7-8 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by **Taylor** (U.S. 6,233,440).

Regarding claims 1 and 7, Fig. 2 of Taylor discloses a radio frequency (RF) linear power amplifier (note: Taylor discloses in col. 1, lines 10-11 that RF power amplifier are typically used

in cellular telephones and other communication devices or see Fig. 1 for detail) operating in an output frequency band, having an output transistor (32), said power amplifier comprising:

(a) a circuit means (31) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier as mentioned in col. 3, lines 44-47; and

(b) a detector circuit means (20/22) for detecting RF input to said amplifier and generating an output signal (between 20 and 22) tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned e.g. in col. 1, lines 51-59, **meeting claims 1 and 7**.

Regarding claim 11, Fig. 2 of Taylor discloses a sliding bias circuit for dynamically controlling quiescent current flowing through an output transistor (32) of a linear power amplifier operating in an output frequency band, said linear power amplifier comprising a circuit means (31) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said sliding bias circuit comprising: a detector circuit means (20/22) for detecting RF input (12) to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned e.g. in col. 1, lines 51-59, **meeting claim 11**.

Regarding claims 2, 8 and 12, Taylor further discloses the linear power amplifier as claimed in claim 1, wherein said circuit means (31) for generating a bias signal producing a quiescent current comprises a differential transistor pair (note: the op amp from numeral 26 inherently comprises a differential pair), said detector circuit means (20/22) output signal being coupled directly to one side of said differential pair as shown in Fig. 2, **meeting claims 2, 8 and 12.**

Claims 1, 5, 7, 11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by **Matsumoto** (U.S. 6,710,649).

Regarding claims 1 and 7, Fig. 6 of Matsumoto discloses a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor (11), said power amplifier comprising:

(a) a circuit means (3) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier as mentioned in col. 2, lines 40-61; and

(b) a detector circuit means (2) for detecting RF input to said amplifier and generating an output signal (see output signal from collector terminal of transistor 24) tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned e.g. in col. 2, lines 25-30, **meeting claims 1 and 7.**

Regarding claim 11, Fig. 6 of Matsumoto discloses a sliding bias circuit for dynamically controlling quiescent current flowing through an output transistor (11) of a linear power amplifier operating in an output frequency band, said linear power amplifier comprising a circuit means (3) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said sliding bias circuit comprising: a detector circuit means (2) for detecting RF input (4) to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned e.g. in col. 2, lines 25-30, **meeting claim 11**.

Regarding claims 5 and 13, Matsumoto further discloses the circuit as claimed in claims 1 and 11, wherein said linear power amplifier comprises first and second power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage, for reducing said quiescent current at a second output stage (note: the term "respective stages" as mentioned in col. 2, lines 31-39), **meeting claims 5 and 13**.

Allowable Subject Matter

Claims 3-4, 6, 9-10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-8577. The examiner can normally be reached on M-F 8-5.

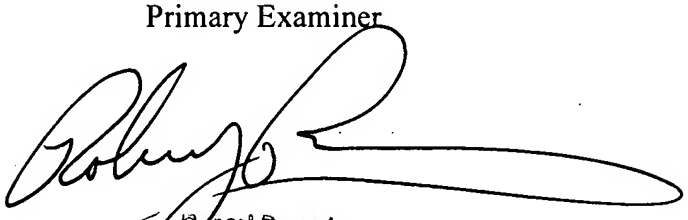
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hieu Nguyen
AU: 2817

hn

Robert Pascal
Primary Examiner



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